Novel Thyristor-Based Microwave Cross-Point Switch MMIC

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***Abstract*—A novel GaAs 16 × 16 cross-point switch monolithic microwave integrated circuit (MMIC) is presented. The switch MMIC incorporates 256 GaAs microwave thyristor devices as switching elements. The thyristors are two-terminal devices with anodes connected to a common horizontal electrode and cathodes connected to a common vertical electrode. Bistable operation of the thyristors permits x–y addressing at the edge of the chip to turn on and off each thyristor. Applications include low-cost low-power high-bandwidth switching of signals for broad-band services. A detailed description of the thyristor device, MMIC structure and design, and simulation and experimental results are presented. Multilayer laminate ball-grid-array package design for the switch matrix will also be explained in detail.**

***Index Terms*—Broad-band communication, millimeter-wave switches, monolithic-microwave integrated-circuit (MMIC) switches, optical communication, packaging, semiconductor device fabrication, semiconductor devices, semiconductor diode switches, thyristors.**

I. Introduction

THERE HAS been considerable progress in recent years in the technology of switching multiple high-bandwidth communication channels within a telecommunication system. A core-switching element, referred to as a switch matrix, routes multiple-input communication signals to multiple-output transmission ports in a reconfigurable manner. Whether the switch matrix is optical microelectromechanical systems (MEMs)- or digital-circuit-based, common requirements include compactness, scalability, low power, switching times of less than 0.1 ms, and high channel-to-channel isolation or low crosstalk. In addition, for high-input/output port count, the switch matrix may be strict sense nonblocking, which means, for instance, any two unused communication channels can be swapped without interruption of any other communication channels that are carrying data [1]. Typically, large-port-count switch matrices are constructed from smaller port count sub-switches. Examples of these are Clos and Spanke large-port-count switch matrices [1]. Digitally based switch matrices have the additional onus of meeting high bandwidth and jitter requirements, especially at OC-192 and OC-768 data rates.

A variety of microwave cross-point switches have been reported in the literature. These include field-effect transistor (FET)-based [2]–[5], MEMs-based [6], and HBT-based [7]–[10] cross-point switches. One of the advantages of using an FET- or HBT-based approach is the ability of providing gain to the switched signal. However, these methods require separate biasing of each switch device or cross-point. This results in circuit complexity and large chip size for even modest port-count switch monolithic microwave integrated circuits (MMICs). Use of x–y addressing (i.e., activation of cross-points using only rows and columns) is, therefore, a necessity. This problem can be addressed by incorporating digital logic circuitry into the switch MMIC. SiGe–BiCMOS technology offers an advantage in this respect. On the other hand, a passive cross-point switch composed of capacitive MEMs switch devices requires no additional digital circuitry for x–y addressing [6]. This is based on the fact that once a capacitive MEMs switch device is turned on, it can be held in the on state by reducing the voltage difference across the plates.

This paper reports on a passive- or analog-based 16 × 16 cross-point switch MMIC employing thyristors [11]. The bistable operation of thyristors enables the x–y addressing without the requirement of extra digital logic circuitry. The simplified circuit schematic of the MMIC is shown in Fig. 1, in this case, with N inputs and M outputs. The pitch of the switching elements is 250 μm in each direction, making the chip size approximately 4.6 mm × 4.6 mm. Analog based means that the MMIC is composed of thyristor switch devices having a conducting (on) state and a high isolation (off) state. Broad-band microwave signals are transmitted through the device in the on state with low insertion loss. In the on state, the thyristor behaves like a p-i-n diode in which electrons and holes flood the intrinsic GaAs layers resulting in high conductivity. In the off state, isolation is determined by depletion-layer thickness of the intrinsic GaAs layers and the resulting capacitance.

The advantage of using thyristors is that on- and off-state control of each device is achieved by the combination of the bistable nature of the thyristor and bias pulses applied to the upper and right sides of the MMIC (see Fig. 1). For an $N \times M$ switch MMIC, there are, therefore, $N + M$ control biases. In the on and off states, the thyristors behave very much like p-i-n diodes.

However, the use of p-i-n diodes instead of thyristors would necessitate $N \times M$ bias controls connected to each p-i-n diode, resulting in extreme circuit complexity. Since p-i-n

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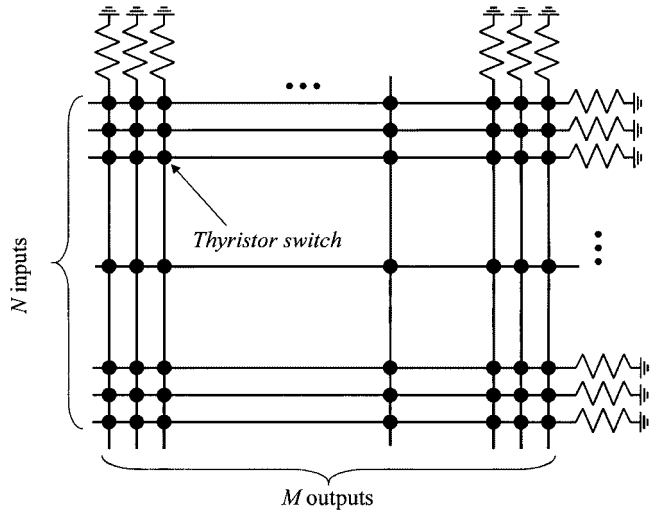

Fig. 1. Equivalent-circuit schematic of an $N \times M$ cross-point switch incorporating thyristor switch devices.

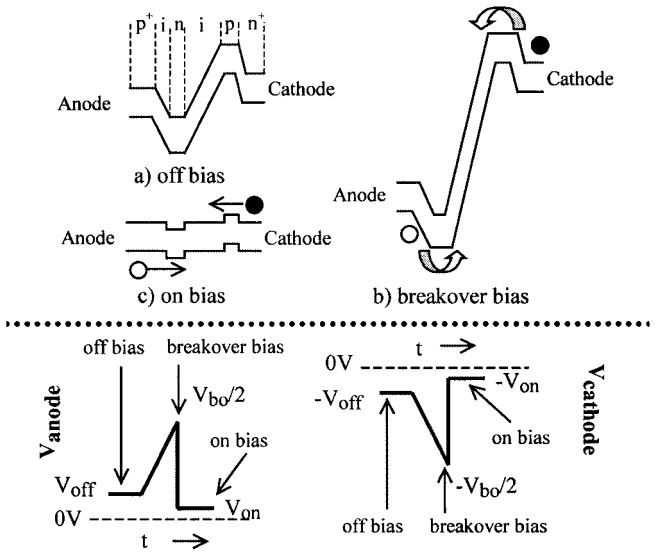

Fig. 2. (*top*) Band diagram of microwave thyristor as the device is turned on and (*bottom*) the respective anode and cathode voltages.

diode switches have been reported to operate from dc to millimeter-wave frequencies near 100 GHz [12], the implication is that a cross-point switch composed of thyristor devices with sufficiently low off-state capacitance can effectively switch with the performance requirements mentioned above at OC-768 data rates.

II. Microwave Thyristor Design

A. Background

Thyristor devices have typically been used for power-switching applications for the past 40 years [13]. A thyristor is characterized by a bistable operation in which the device becomes conducting when a voltage difference applied between the anode and cathode exceeds the break-over voltage. For power devices, the break-over voltage is determined by onset of avalanching within the device.

The microwave thyristor described here is composed of a p^+-i-n-i-p-n^+ GaAs epitaxial stack grown on a semi-insulating substrate. Device isolation is achieved by a wet etch in which 20-μm-diameter mesas are formed on a 250-μm pitch. An applied bias across the epitaxial stack results in depletion of the n-i-p junction and eventual reach through of the N-layer provided $N_d < N_a$. At this point, a reduction of the built in potential of the p^+-i-n junction occurs and holes are thermionically transported to the p region of the device that behaves much like the base of a transistor. The p-n^+ junction becomes forward biased, at which point electrons are injected into the intrinsic layers. The device is now in a state in which more and more holes and electrons flood into the central portion of the thyristor. The potential between the anode and cathode collapses to a value comparable to the turn on voltage of a p-i-n diode. Silvaco BLAZE simulations show that this process takes approximately 2 ns. Note that the break-over voltage is determined by the reach through voltage of the n-layer that is controlled by doping level and thickness. The off-state device capacitance is separately controlled by thickness of the two intrinsic layers.

Fig. 2 depicts the transient process for turn on. Note that voltage pulses must be applied simultaneously to both anode and cathode to achieve turn on. An adjacent thyristor along the same horizontal or vertical axis shown in Fig. 1 experiences a potential increase of $V_{\rm off} + (V_{\rm bo}/2)$ that is insufficient for turn on. The device is reverted to the off state by applying pulses to ground. The thyristor device was designed for an off-state capacitance C_{oj} of 15.8 fF and the typical on-state series resistance R_s was 5.7 Ω.

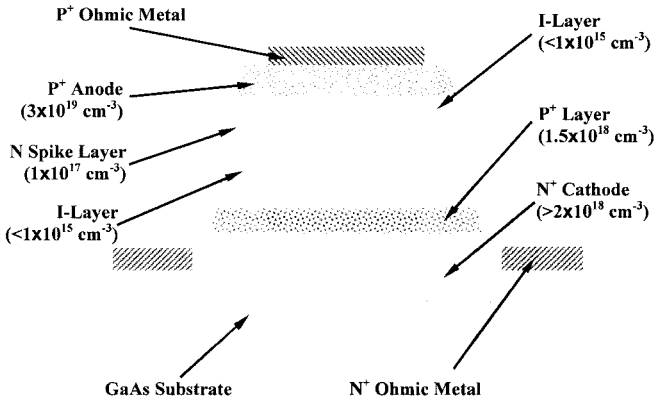

Fig. 3. Millimeter-wave GaAs thyristor structure.

B. Growth Technique

Growth of the thyristor epitaxial films was accomplished in the M/A-COM, Lowell, MA, low-pressure metal–organic vapor phase epitaxial (LP-MOVPE) reactor. The selection of growth parameters required to manufacture this device centered on the need to maintain thickness control of individual layers with minimal transition broadening between layers. In addition, it was required to maximize carbon incorporation while minimizing effects of hydrogen passivation. A cross section of the epitaxial stack is shown in Fig. 3. The growth sequence of the $p^+ - i - n - i - p - n^+$ thyristor structure starts with deposition of a 2-μm N^+ layer, heavily doped with silicon at 5×10^{18} cm^{-3}, on a M/A-COM produced semi-insulating substrate. This first layer served as the cathode

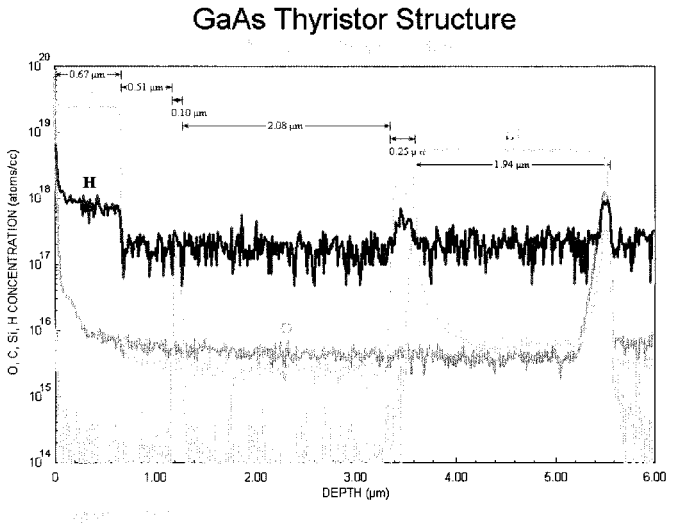

Fig. 4. SIMS profile of the millimeter-wave GaAs thyristor. The low concentrations of oxygen and hydrogen are indicative of a high-quality film.

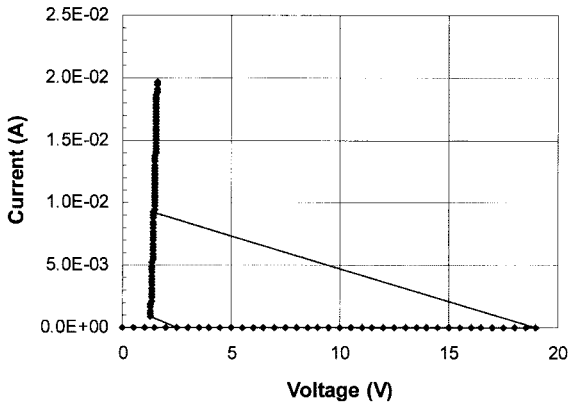

Fig. 5. DC characteristics of the microwave thyristor showing the break-over voltage ($V_{\rm bo}$) and holding current ($I_{\rm hold}$).

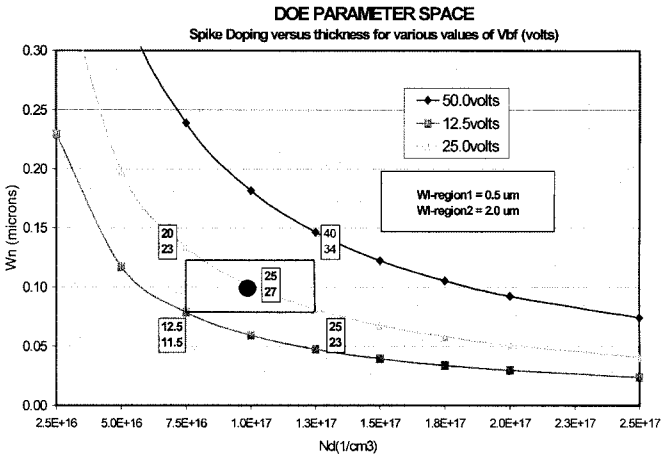

Fig. 6. Results of the DOE designed to investigate break-over voltage versus spike layer parameters.

contact. The next layer is a 0.2-μm carbon-doped P-layer at 1.5×10^{18} cm^{-3} forming the first of the three junctions. The next three layers are a 2-μm unintentionally doped I-layer, an n-type silicon-doped spike layer, and a 0.5-μm I-layer. The final layer in the epitaxial stack is a 0.7-μm P^+ layer heavily doped with carbon at 3×10^{19} cm^{-3}. This top layer served as the anode contact to the device. It was observed that the P^+ layer and the N-spike layer are the most critical layers in determining the dc characteristics of the thyristor.

In examining the secondary ion mass spectrometry (SIMS) profile, shown in Fig. 4, it can be seen that the oxygen signal throughout the structure is in the noise level and the hydrogen content in the P^+ anode layer is less than 3% of the total impurity content. The low concentrations of oxygen and hydrogen are indicative of a high-quality film. The transition width of the n-type spike layer, sandwiched between the two I-layers, is well under 200 Å.

C. Thyristor DC Characterization and Design of Experiment (DOE)

As described previously, thickness W_n and carrier concentration N_d of the spike layer determines the thyristor break-over voltage. These parameters were varied as part of a simple DOE. A total of five doping and thickness combinations were used in the DOE to examine dependency of the forward break-over voltage $V_{\rm bo}$ on the resulting spike doping $N_d \times W_n$. Simple mesa structures were fabricated with top and bottom metal contacts to measure break-over voltage and holding current. A typical dc characteristic of the thyristor is shown in Fig. 5. The break-over voltage and holding current for this particular device are 18 V and 1.0 mA, respectively.

Fig. 6 shows three theoretical constant $V_{\rm bo}$ contours as a function of W_n and required doping N_d. The break-over voltage was characterized for each of the five samples and is designated by white outlined boxes in the figure. This agreement shows that doping and thickness calibration of the reactor prior to growth was sufficient for manufacturing thyristors with a specific design value of break-over voltage. In this study, a spike doping of 9.4×10^{11} cm^{-2} was chosen with an associated $V_{\rm bo}$ of 24.7 V.

D. Thyristor S-Parameters and Equivalent Circuit

Microwave probeable series connected thyristors were fabricated using process techniques essentially identical for the fabrication of conventional series connected p-i-n diode test structures. This involved formation of an air bridge to the top cathode contact and a surrounding bottom metallization to the anode contact. Ground–signal–ground microwave probeable pads permitted on wafer measurement of S-parameters from 0.05 to 40 GHz. A physically plausible equivalent circuit was generated in ADS to fit the measured data of the test structure. These results are shown in Fig. 7 for a 20-μm-diameter thyristor and show that the fit is quite good. In the on state, return loss of the thyristor is better than 20 dB up to 50 GHz. Insertion loss is better than 0.5 dB at 10 GHz and 1 dB at 50 GHz. In the off state, the thyristor has an isolation of better than 20 dB at 10 GHz.

Parasitic via inductance and lead capacitance to the thyristor was removed from the test structure equivalent circuit to obtain the deembedded equivalent circuit of the bare thyristor shown in Fig. 8. An off-state capacitance of 15.8 fF and an on-state series

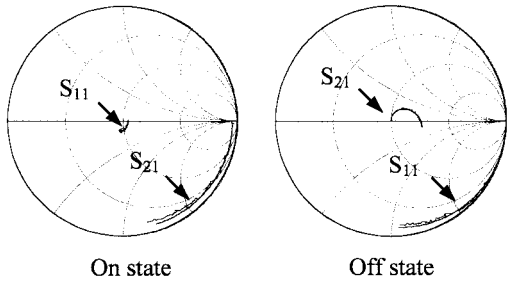

Fig. 7. Measured and equivalent-circuit S-parameters from 0.05 to 40 GHz of a 20-μm-diameter series connected thyristor.

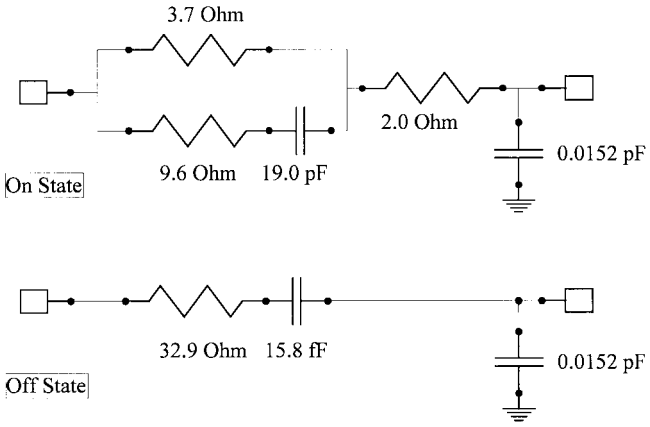

Fig. 8. Deembedded on- and off-state series thyristor equivalent circuits. Off-state capacitance is 15.8 fF and on-state resistance is 5.7 Ω. These values are comparable to the state of the art p-i-n diodes of the same geometry.

resistance of 5.7 Ω show that the thyristor behaves like a p-i-n diode under equivalent bias conditions. These equivalent-circuit models were subsequently used in the design of the 16 $\times$ 16 and 16 $\times$ 32 cross-point switch matrix die.

III. Design of the Cross-Point Switch MMIC

A. Fabrication of the MMIC

The MMIC has been fabricated on a 100-μm-thick semi-insulating GaAs substrate using benzocyclobutene (BCB) microstrip transmission lines on a 250-μm pitch ($\sim$10 mil). Construction of the MMIC is pictorially depicted in Fig. 9, which shows thyristors and interconnecting transmission lines. Fig. 10 shows typical dimensions of the thyristor mesa. A representative cross section of the MMIC is also shown in Fig. 11. Construction of the switch MMIC can be briefly described as follows. The first step is to grow thyristor epitaxial layers on the GaAs substrate, as explained earlier.

After mesa isolation of the thyristor devices, a metal ground plane is deposited over the etched area with openings for the thyristor mesa. A 5-μm BCB layer that acts as the substrate for the microstrip interconnects is then spun on the wafer and cured. The BCB around the thyristor is then removed and air bridges are fabricated to connect horizontal and vertical transmission lines to the anode and cathode of the thyristors. An overlay of BCB is then spun on and cured for passivation and to back fill the air bridges.

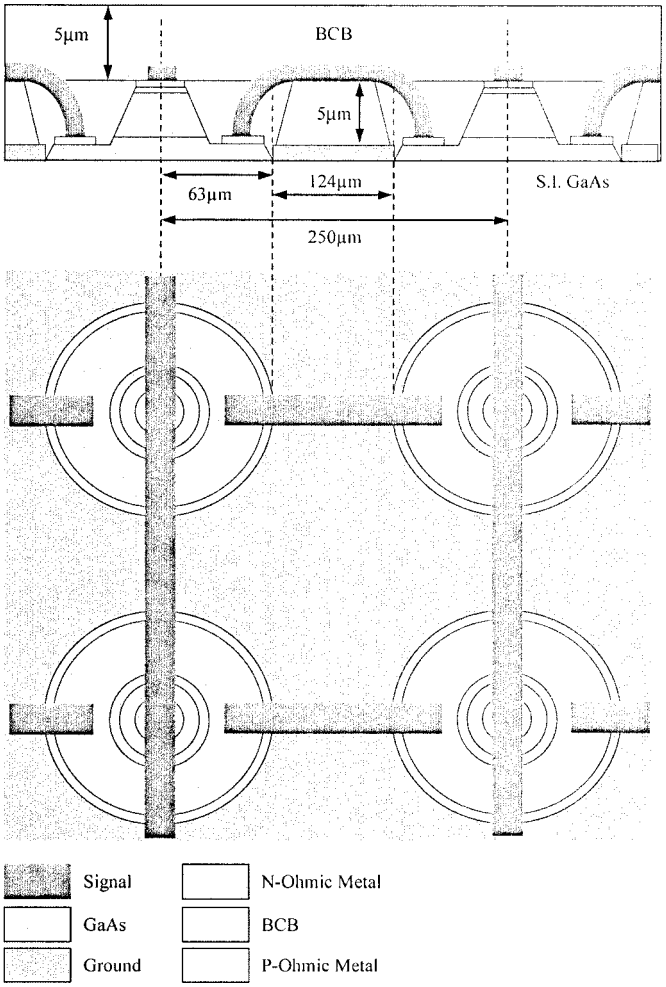

Fig. 9. Layout of the GaAs thyristor cross-point switch. Note that this figure is not to scale.

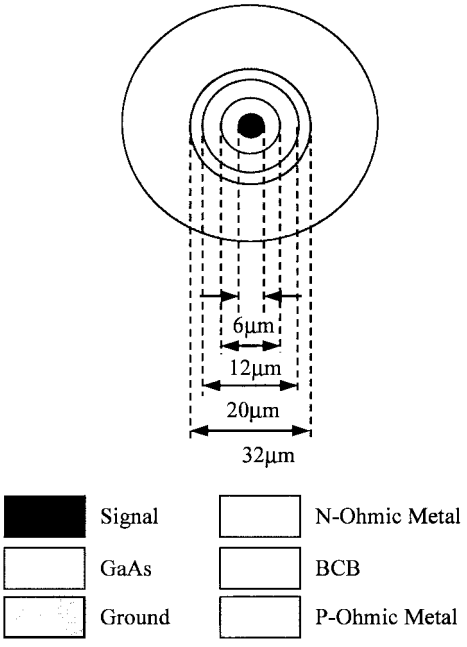

Fig. 10. Typical dimensions of the thyristor mesa. Note that this figure is not to scale.

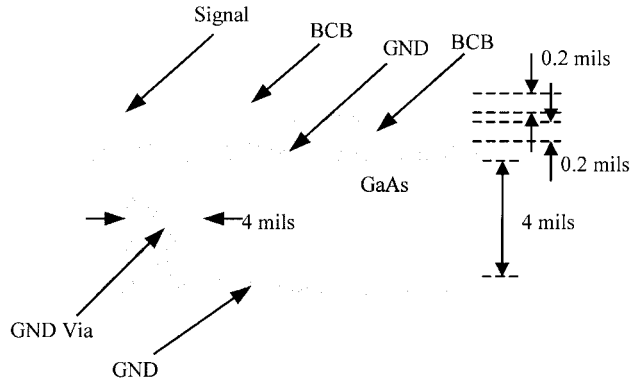

Fig. 11. Representative cross section of the MMIC showing BCB microstrip lines. Note that this figure is not to scale.

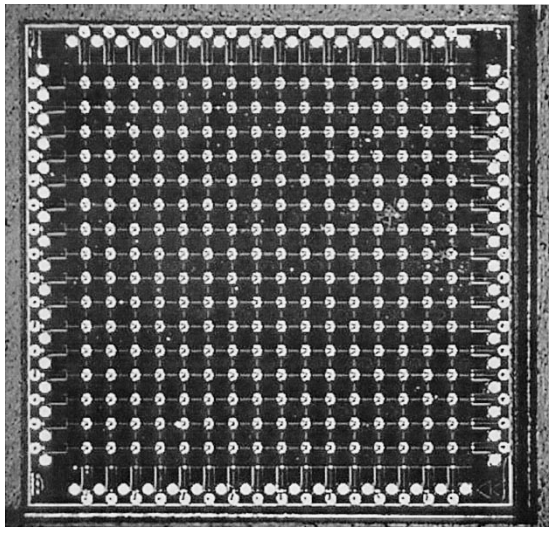

Fig. 12. 16 × 16 thyristor cross-point switch die. Dimensions of the die are 4.6 mm × 4.6 mm.

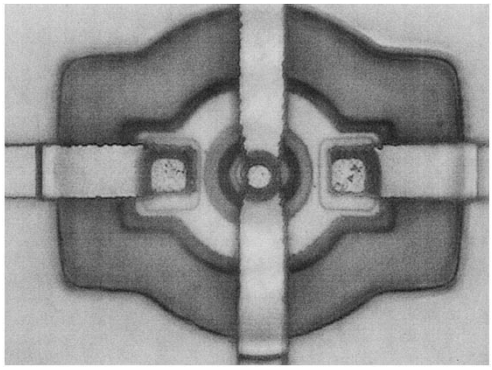

Fig. 13. Enlarged view of the thyristor junction. Notice the ground plane opening around the mesa.

The dimensions of the die for 16 × 16 and 16 × 32 MMICs are approximately 4.6 mm × 4.6 mm and 4.6 mm × 5.9 mm, respectively. Manufactured 16 × 16 cross-point switch die and an enlarged view of the thyristor switch device are shown in Figs. 12 and 13, respectively. Thyristor switches are clearly visible at each cross-point. Note that the MMIC die has grounding via-holes next to every bonding pad to provide the shortest path for RF ground currents.

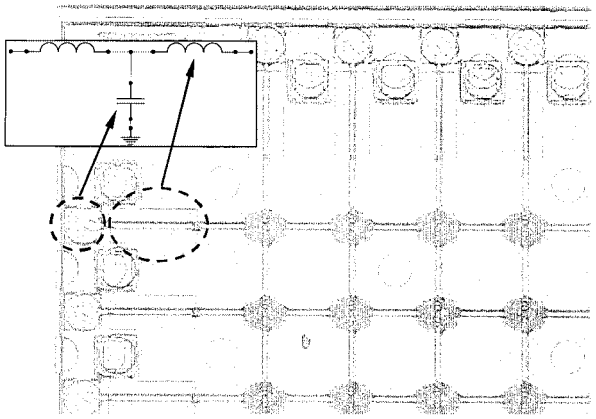

Fig. 14. Cross-point switch die showing the low-pass filter networks for wire-bond compensation. The inset figure depicts the low-pass topology with corresponding layout sections. Leftmost inductor corresponds to wire bonds.

B. Design of the Transmission Lines

An important feature of the MMIC design is the use of microstrip lines on BCB instead of GaAs. In other words, a 5-μm BCB layer was used as substrate for the microstrip lines instead of the 100-μm-thick GaAs substrate. This allowed very narrow (12-μm) 50-Ω transmission lines that would not be possible otherwise on top of a thick GaAs substrate. In fact, the combination of periodic thyristor capacitance and transmission-line interconnects for any row or column of the MMIC forms an artificial transmission line. The periodic capacitance of the thyristors are absorbed by a reduction in interconnect transmission linewidth from 12 to approximately 10 μm. A close-up picture of the 16 × 16 cross-point switch MMIC is shown in Fig. 14. Note that the circuit has low-pass filter structures for each input and output to compensate the wire-bond inductances. One way of compensating the wire-bond inductance is to design a T-type *L–C–L* low-pass network where the wire-bond inductance is one of the inductive elements [14]. Using the area under the wire-bond pad can conveniently create the capacitive term of the network. Note that since the pad area is relatively large and dielectric thickness is small (5 μm), the wire-bond pads create a significant capacitive loading.

The remaining task is to create another inductive term after the wire-bond pad. However, because the width of 50-Ω transmission lines is already at photolithographic limits of the process, additional means were required to create an inductive section. Therefore, it was decided to remove some portions of the ground plane at each transition to increase the inductance of the microstrip lines, as shown in Fig. 14.

Reduced transmission interconnect linewidth by the use of a 5-μm-thick BCB substrate was also extremely crucial in the consideration of horizontal line-to-line and vertical line-to-line coupling. Far-end microstrip line-to-line coupling is exacerbated by a large difference in dielectric constants between the substrate on which the microstrip resides and the overlaying dielectric constant due to an increased difference in the even- and odd-mode phase velocities. Since the dielectric constant of BCB is 2.7, the even- and odd-mode phase velocities are closely matched resulting in reduced far-end coupling. On the other hand, near-end coupling is reduced by the large

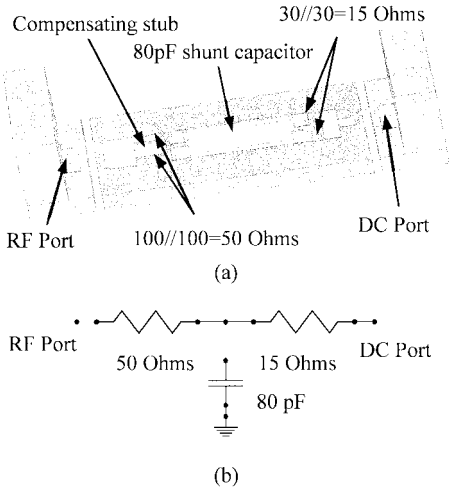

Fig. 15. (a) Perspective view of the bias-tee circuit. (b) Equivalent topology [15]. Note to the elongated shunt MIM capacitor (see the text).

pitch-to-microstrip linewidth ratio of 25. Simulations with ADS show that far-end coupling is -60 dB up to 40 GHz for two 50-Ω transmission lines on BCB with 10-mil pitch and 4.6-mm length and near-end coupling is -70 dB. It was found that the array channel–channel isolation and crosstalk is dominated by coupling through the off-state thyristor capacitance.

C. Cavity Resonance Modes in the GaAs Substrate

Potential cavity resonance in the GaAs substrate was another important issue. As can be seen in Fig. 11, there are two ground planes on the top and bottom surface of the GaAs substrate. There are also ground via-holes along the periphery of the die to bring up the ground currents from the bottom ground plane to the ground plane of the microstrip lines. This configuration forms a rectangular cavity where resonance modes can be excited in the frequency band. Since there are ground-plane openings under the inductive portion of the input and output matching networks, as well as at the base of each thyristor, potential coupling between microstrip lines and the cavity formed beneath them exists. Therefore, additional GaAs substrate vias with 20-mil pitch across the whole die were fabricated, thereby shorting the vertical component of the electric field and suppressing any resonance mode.

D. Design of the Bias Tee

As stated previously, the matrix transmission lines must be terminated properly, as depicted in Fig. 1, to avoid reflected power from the top and right edges of the matrix that would deteriorate the transmitted output signal. In addition, dc control pulses must be injected to the matrix through rows and columns to activate thyristors. To accomplish both purposes a bias-tee circuit using M/A-COM's heterolithic microwave integrated circuit (HMIC) process was designed and is shown in Fig. 15. HMIC is a patented process that joins two different materials, low-loss glass and silicon, into one monolithic substrate. This technique enables the creation of microwave and millimeter-wave circuity integrating all required passive components, including resistors, high-Q inductors and capacitors, and controlled impedance transmission lines.

Each column and row in the switch matrix is terminated with this network, as shown in Fig. 1. Note that these bias-tee circuits are separate circuits that need to be connected with the matrix during assembly. The most critical aspect of this design is the elongated metal–insulator–metal (MIM) shunt capacitor placed on a long ground pedestal; enabled by M/A-COM's HMIC process. This circuit approach allows high dc-RF isolation without the requirement of bulky MIM inductors. The series resistors in the dc current path drop approximately 0.65 V for a nominal thyristor current of 10 mA in the on state. Details of the bias-tee design will not be discussed further in this paper. However, interested readers are referred to the literature on the design [15].

IV. Packaging

A. Background

Ball-grid-array (BGA) technology has been selected to package the switch matrix since it offers low-insertion loss at millimeter-wave frequencies and modularity. BGA packages can provide high-density I/O in a robust packaging environment. They are also preferable in high-volume automated manufacturing due to compatibility with pick-and-place assembly capability. Ceramics are the most often used materials to build high-frequency BGA packages [16], [17]. Alumina, high-temperature co-fired ceramics (HTCCs), and low-temperature co-fired ceramics (LTCCs) are examples of different ceramic materials that can be used in designing such packages. The main problem with the ceramic materials is that the coefficient of thermal expansion (CTE) is significantly different from the CTE of nearly all polymer and polymer-composite laminate printed circuit boards (PCBs). This poses a difficulty in mounting large ceramic BGA packages on the host PCB made of laminate boards. This is because standard size ball contacts nearly always develop cracks after thermal cycling unless additional precautions such as underfill are used. These cracks eventually result in open-circuit failure by disconnection of the signal lines. For example, CTE of alumina is 6.7 °ppm/C, whereas CTE of FR4 is 16 °ppm/C. Since solder melts at 183 °C, cooling to ambient after reflow creates a mismatch of $(16-6.7)\times(183-25)$, or 1470 ppm per unit length, which is a significant amount. The CTE mismatch in this case should not exceed 2–2.5 ppm for adequate reliability (see Fig. 16).

It should also be mentioned that there are some new ceramic materials introduced recently that have comparable CTE with the laminate materials, such as Kyocera high thermal coefficient of expansion (HITCE) LTCC. These materials have favorable electrical properties for millimeter-wave package design. For instance, dielectric constant and loss tangent for Kyocera LTCC GL550 are 5.7 and 0.002, respectively, at 60 GHz. However, these materials have expensive tooling costs and long procurement time, which might be a consideration. For this application, we designed packages using both laminate materials and HITCE LTCC, but in this paper, we are reporting the results of the former. To the authors' knowledge, the use of multilayer laminate materials in a millimeter-wave package has not been reported before in the way we are demonstrating here.

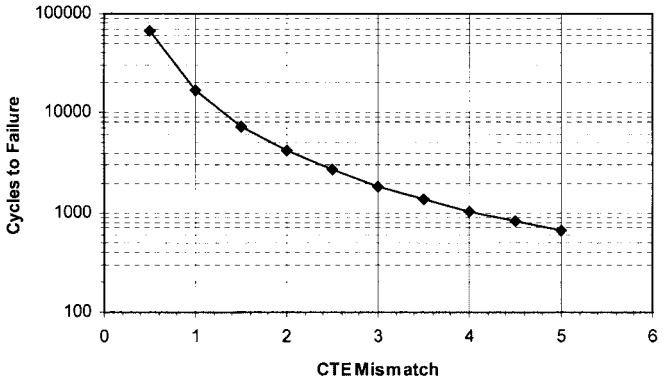

Fig. 16. Cycles to initial failure versus CTE mismatch for $-65\,^{\circ}$C to $+125\,^{\circ}$C in a 20×20 mm^2 package. At roughly 2–2.5 ppm CTE mismatch, the value drops below 5000 cycles [18].

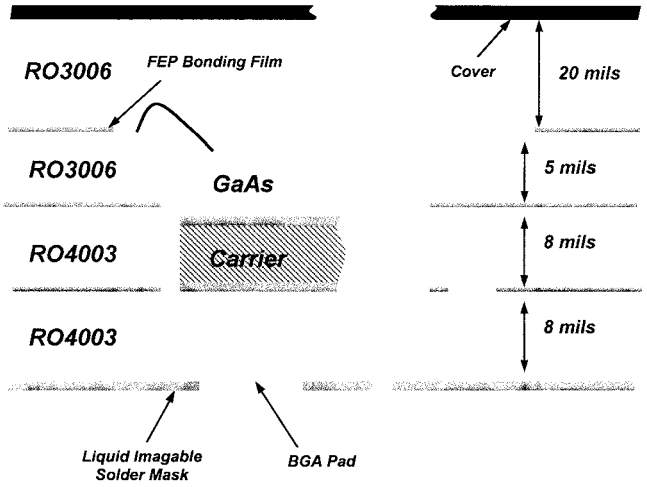

Fig. 17. Layer stack-up of the multilayer laminate BGA package showing the MMIC cavity.

B. Design Considerations

Due to package size and cost considerations, laminate materials have been used to design a multilayer BGA package (see Fig. 17). Several mechanical and electrical features of the package design were first considered before the final optimization by full-wave electromagnetic simulation. First, the package required a multilayer construction to permit easy creation of cavities in the package. Second, use of laminate materials would minimize the CTE mismatch problem for large packages, as explained before. Third, a dielectric cover layer bonded over the microstrip transmission lines to improve isolation by reducing line-to-line forward coupling. The cover layer equalizes even- and odd-mode phase velocities of a coupled line pair because a microstrip line is not a true TEM transmission line. A side benefit of this is simplified sealing with a cover plate. Fourth, the BGA transitions were designed to minimize the series parasitic inductance by placing BGA balls directly on top of via-holes after filling the holes with a suitable conductive material.

The success of the package design hinged on performance of the BGA electrical transitions. It is known that BGA transitions present significant series inductance that deteriorates return loss of the circuit at high frequencies. Series inductance of the BGA transition is usually compensated by placing ground

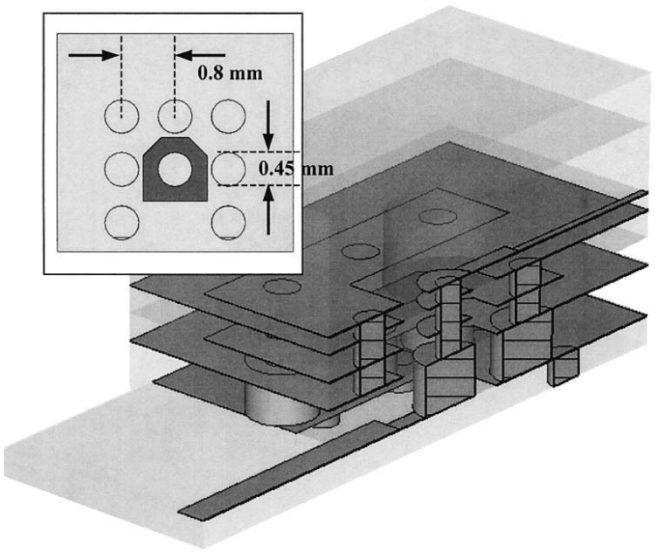

Fig. 18. Sliced-through view of the BGA transition. The center signal conductor and surrounding ground via-holes are clearly visible. The inset figure shows the bottom view of the BGA transition.

vias around the signal via-hole. This increases the shunt capacitance to ground. This structure can be viewed as a quasi-coaxial structure along the BGA transition [19]. Since the characteristic impedance of a loss-free TEM transmission line is given by the equation $Z_0 = \sqrt{L/C}$, increased shunt capacitance compensates the increased series inductance making Z_0 close to 50 Ω. Adjustment of spacing between the center and ground vias, as well as via diameters, accomplishes this. The permittivity of the substrate materials affects this adjustment. It was found that optimum performance is obtained when the via-holes in the dielectrics and the BGA balls are aligned. In other words, the BGA balls are placed directly on to the vias in the dielectrics. On the other hand, placing the balls directly on top of vias poses a problem, which is given as follows: the molten solder of the balls tends to flow into unfilled plated via-holes when the bumps are reflowed. To prevent this, all via-holes directly beneath the BGA balls must be pre-filled using solder or any other appropriate material such as a curable conductive polymer (e.g., Dupont CB100). As noted, aligning the balls with via connections is especially important for package performance. On the host PCB, grounding via-holes can be offset with respect to the BGA balls to eliminate the via-hole filling for the host PCB, thus reducing cost. Fig. 18 shows a cross section of a single BGA transition incorporated in the package design.

A photograph of the package is shown in Fig. 19. The package size is 35 mm $\times$ 35 mm with a thickness of approximately 2.0 mm. BGA ball diameters and pitch were chosen to be 0.45 and 0.8 mm, respectively, to minimize the package footprint. The frequency bandwidth of the package is dc to 40 GHz. It can accommodate up to 48 high-frequency I/O and 48 dc connections for RF and control signals, respectively, on a single-layer host board.

Fig. 20 shows the uncovered package containing the switch matrix die mounted on a test board. The two dies on the top and right are bias-tee circuits, which are used to inject control signals to activate each junction. Test results of the BGA

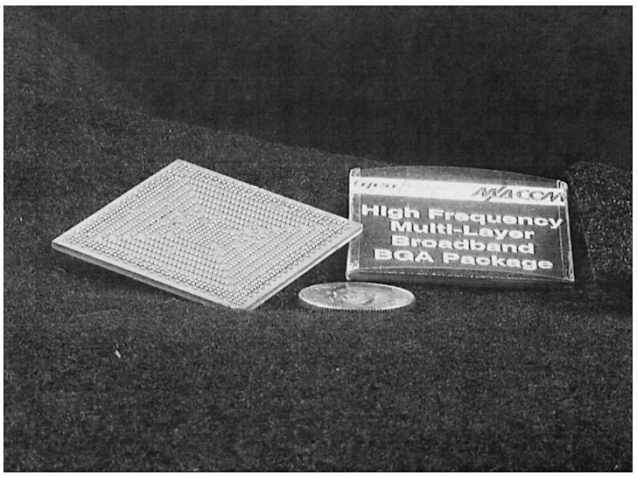

Fig. 19. 16 × 16 BGA switch-matrix package. BGA ball diameters and pitch are 0.45 and 0.8 mm, respectively.

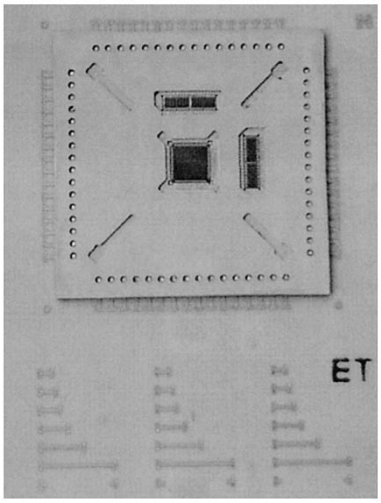

Fig. 20. 16 × 16 switch matrix mounted on a test board. The MMIC at the center is the thyristor GaAs switch. The two dies on the top and right are the bias-tee circuits.

package are given in Fig. 21. The measurements are for two back-to-back BGA transitions connected through a microstrip line implemented on a special test package. Insertion loss of the whole package including two BGA transitions is less than 1 and 4 dB at 10 and 40 GHz, respectively.

V. Cross-Point Switch Operation

For nonbroadcast operation of the thyristor cross-point switch, exactly one thyristor is turned on per row and corresponding column. Activation of a thyristor cross-point is depicted in Fig. 22. Note that only the junction at the intersection of the pulses will be activated because combined application of voltage pulses exceeds the break-over voltage. This mechanism extremely simplifies the bias line distribution and it is one of the advantages of the thyristor cross-point switch.

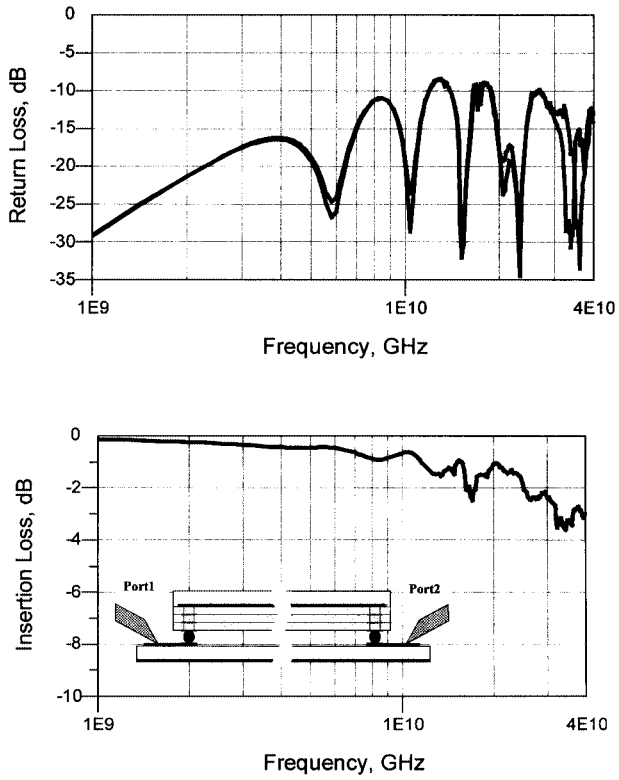

Fig. 21. Return and insertion losses of the multilayer BGA package. Two BGA transitions connected back-to-back via a 11-mm-long transmission line is measured. The inset figure shows the measured configuration.

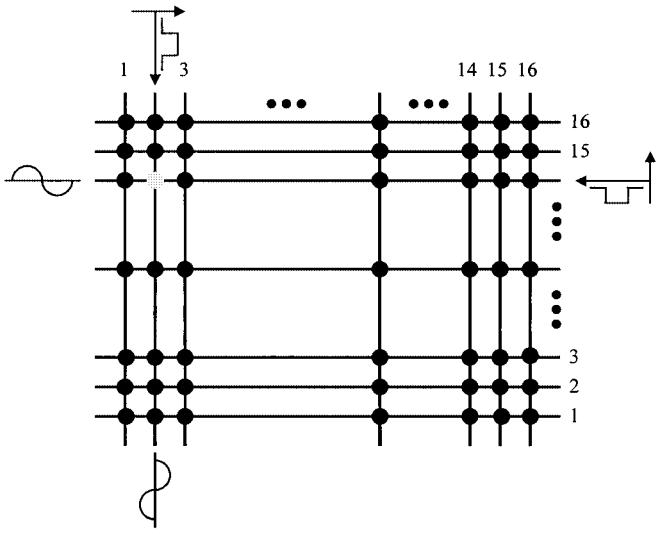

Fig. 22. Activation of a junction in the thyristor cross-point switch. Note that only the junction at the intersection of the pulses will be activated because the combined voltage pulses exceed the break-over voltage.

The input signal on the left of Fig. 22 propagates along the horizontal transmission line and scatters in four directions at the thyristor, which is effectively a point contact short with the vertical transmission line. Power scattered to the top and right edges of the chip must, therefore, be absorbed by a 50-Ω termination in order to eliminate time-delayed versions of the original signal at the output. These 50-Ω terminations, currently off-chip, must also have the capacity of passing low-frequency thyristor bias control pulses.

Due to these terminations, the nominal insertion loss at the output of the switch array for any path is, therefore, 6 dB. Any losses due to connectors, package, and PCB transmission lines would be in addition to this. For broad-band SONET signals, frequency-dependent losses introduce eye closure and jitter on the output signal. Equalizing circuitry and regeneration–reshaping–retiming (3R) post processing can recover the signal even with 10-dB frequency-dependent losses from dc to the upper cutoff frequency of interest.

Thyristor addressing of the switch matrix is achieved with a single current source composed of discrete transistors multiplexed to the bias tees through a 1×16 switch mounted on a PCB. There are two such current sources of opposite polarity for the anode and cathode sides of the matrix or the upper and right edges in Fig. 22. These current sources provide 10 mA across shunt 22-nF capacitors (which also extends the lower frequency cutoff of the bias tees). This translates to approximately 1-V/μs voltage ramp across the anode and cathode of the thyristor. In approximately 10 μs, the thyristor, with a nominal break-over voltage of 20 V, is turned on. A maximum of 34 V may be applied depending on the thyristor break-over voltage. Once the thyristor is activated, current is drawn from a separate voltage source through a diode to keep it on. A 10-μs turn-on time was sufficient for our application. Although there are many ways to provide bias, it was found that activation by current sources was a simple and efficient way of providing bias to thyristors, which may vary in break-over voltage across the die and from die to die.

VI. Measurement Results

Break-over voltage and holding current uniformity across the 16×16 cross-point switch MMIC were characterized using an automated test station. Fig. 23 shows that excellent uniformity of break-over voltage and holding current are achievable even with a large die size of 4.6×4.6 mm. A uniform break-over voltage of 20 V and holding current of 1.2 mA is achieved. Similar statements for an even larger 16×32 switch die also apply.

A prototype PCB, shown in Fig. 24, was designed in order to test RF performance of the switch. Corning Gilbert, Glendale, AZ, GPPO series connectors were used at the PCB to allow connection to 16 inputs and outputs. Fig. 25 shows the resulting typical output eye diagram for an input signal consisting of an OC-192 SONET $2^{23} - 1$ pseudorandom bit sequence (PRBS). The bit error rate (BER) was better than 10^{-14}. The eye diagram quality can be significantly improved by the use of a 10-GHz limiting amplifier from GTRAN, Newbury Park, CA, at the PCB output. Fig. 26(a) shows a typical insertion loss for path $(1, 15)$, which is the second input from the top of the array and last output. Note there is a slope of 3–4 dB from 0.05 to 12 GHz that is mostly due to PCB and package trace loss. Fig. 26(b) shows the isolation when this path is turned off. The on/off insertion-loss ratio is greater than 26 dB at 10 GHz and 40 dB at 1 GHz.

Bias pulses generated by reconfiguration of the matrix cannot disrupt signals on adjacent outputs in order to achieve nonblocking operation. As discussed previously, the voltage across the thyristor collapses in approximately 2 ns, resulting

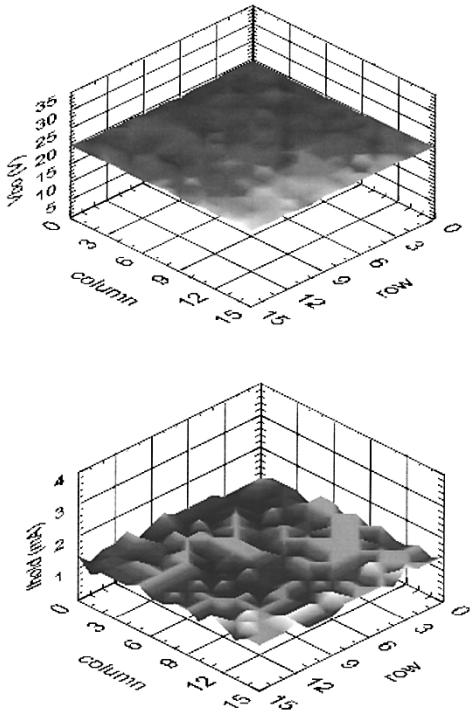

Fig. 23. Variation of the: (*upper*) break-over voltage $(V_{\rm bo})$ and (*lower*) holding current $(I_{\rm hold})$ across the 16×16 switch matrix MMIC die.

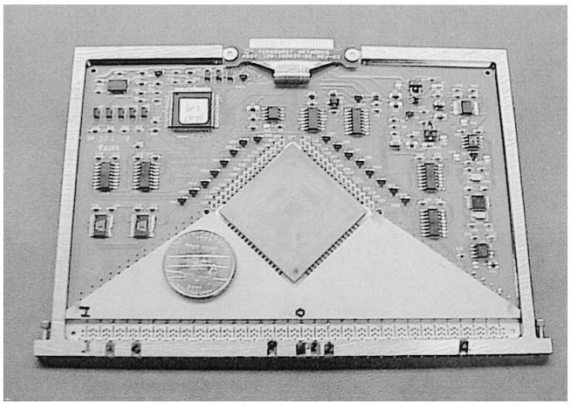

Fig. 24. Prototype PCB incorporating the packaged switch of Fig. 19.

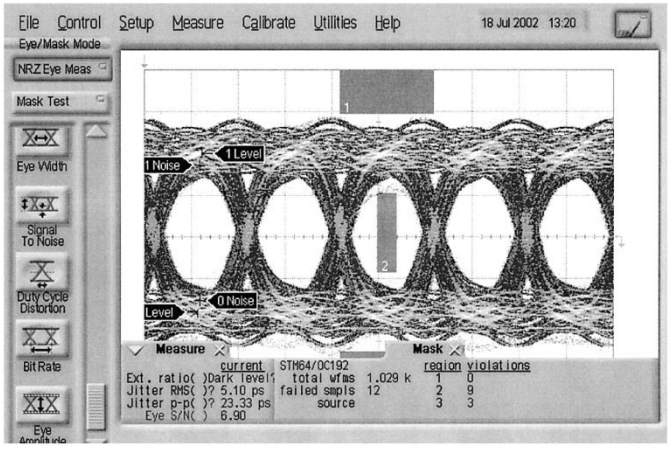

Fig. 25. Output eye diagram of path $(1, 15)$ of the PCB shown in Fig. 24 $(\text{BER} < 10^{-14})$.

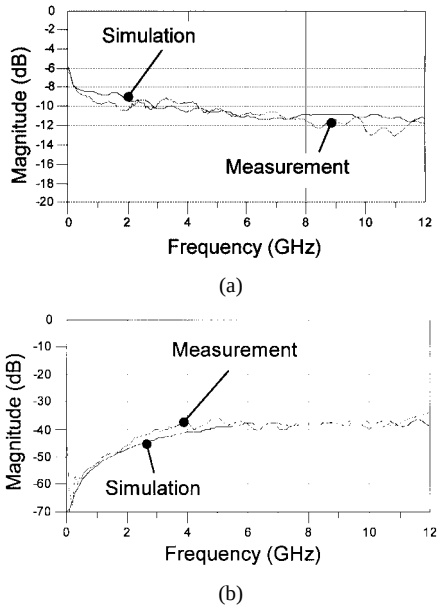

Fig. 26. (a) On insertion loss of path $(1, 15)$ of the PCB shown in Fig. 24. (b) Off insertion loss of path $(1, 15)$ of the PCB shown in Fig. 24.

in a voltage pulse of this width. However, as seen in Fig. 26(b), isolation at subgigahertz frequencies is approximately 60 dB, resulting in significant attenuation of any feed-through pulse. It was found experimentally that, with a typical multiplexed SONET input signal of 250 mV, the signal-to-noise ratio was still 20 dB during a reconfiguration event, resulting in no bit errors and, therefore, nonblocking operation. For input signals significantly lower than 250 mV, pre-amplification should be employed.

VII. Conclusion

A novel compact GaAs 16 $\times$ 16 cross-point switch MMIC utilizing microwave thyristors has been presented for the first time. Multilayer high-frequency laminate BGA package development has also been reported.

The pitch and size of the die is largely determined from package fabrication constraints. Further improvement in the resolution of packaging technology will permit a smaller die size. While low BER transmission of OC-192 SONET signals has been demonstrated, a further reduction of thyristor capacitance will result in a MMIC that is operational at OC-768 data rates. This is preferable to FET or HBT approaches that require smaller device feature size. Although the MMIC was originally designed for optical systems, it can be used in any low-power millimeter-wave switching application that requires high density.

M/A-COM was able to achieve 50% chip yield at the end of the project timeline. A principal limiting factor affecting chip yield was the use of contact-mask photolithography instead of a stepper. Further refinement of the process steps in addition to employment of a stepper would further increase the yield.

Teraburst has constructed a 256 $\times$ 256 three-layer Clos switch matrix utilizing 16 $\times$ 16 and 16 $\times$ 32 switch matrix PCBs, as shown in Fig. 24. The use of GPPO edge connectors on each PCB permitted a compact realization of this switch matrix of only 9 in $\times$ 5.5 in $\times$ 11 in. Inter-stage passive equalization circuits were used to compensate for frequency-dependant losses throughout the switch. These circuits are visible at the bottom edge of the PCB in Fig. 24. Since inter-stage amplification was not employed in the switch matrix, attenuation was approximately 40 dB. However, this still provided over 20 dB of margin above the thermal noise floor with a SONET input signal of 250 mV. Experimentally it was determined that OC-48 signals could be recovered with as much as 65-dB attenuation with low-noise amplification. It was found that great care in all transition designs was required to minimize insertion-loss ripple and deviations in linear phase that degrade the output eye-diagram quality. OC-48 signals were successfully transmitted through the switch with no bit errors for at least two days. Good output eye diagrams with OC-192 input signals were also obtained, but further characterization was not completed.

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Elim Chan, photograph and biography not available at time of publication.

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His research interest included the investigation of induced fields in human bodies at power frequencies with Brunel University, Uxbridge, U.K. He then joined the University of Limerick, where he was a Post-Graduate Researcher involved on a project involving prediction of radiated fields in relation to cavity resonances and aperture excitation in computer workstations, which was supported by Sun Microsystems in order that Federal Communications Commission (FCC) regulation are complied with. He also extended the dipole moment method to include resonating apertures in conjunction with resonating enclosures in predicting radiated fields. In April 2001, he joined the Corporate Research and Development Department, M/A-COM, Lowell, MA, as a Senior Engineer, where his main responsibilities are electromagnetic analysis, modeling, and design of RF and microwave passive and active devices and circuits. He has authored or coauthored six conference publications He has three patents pending.

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